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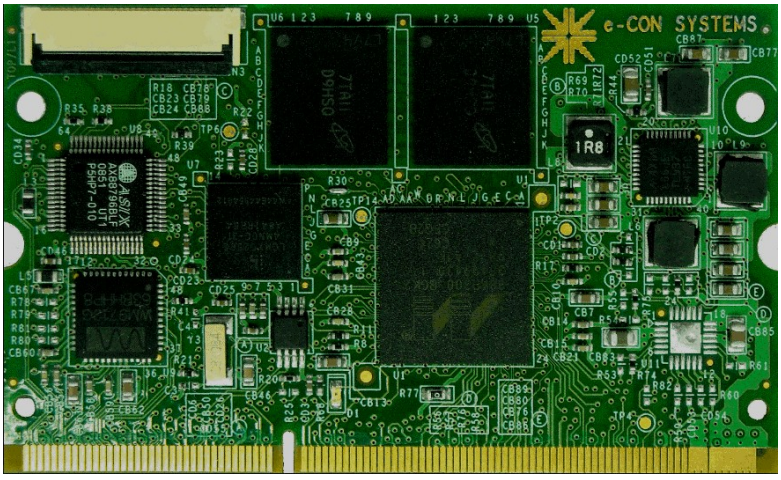
eSOM300



Data Sheet

Revision 1.2
14-April-2010

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Revision History

Rev No	Date	Major Changes	Author
1.0	12-Jan-2010	Initial Release	Ranjithkumar M
1.1	14-April-2010	- Added mechanical description - Corrected pin description and SODIMM Pin Numbers - Added power specification	Ranjithkumar M

Introduction

e-con Systems has developed low power Computer/System-on-Module, eSOM300, based on PXA300 CPU with the very basic peripherals in a compact form factor. The eSOM300 has PXA300 CPU running up to 624MHz, mobile DDR SDRAM configurable from 64MB to 256MB, NAND flash configurable from 256MB to 1GB, 10/100 Mbps Ethernet Controller, Audio Codec and Battery Charger. The eSOM300 module also has the Power Management IC that can be programmed through I2C to implement DFM and DVM. The configuration has been chosen in such a way to address the complete range of applications based on 32-bit XScale processor. The module comes with Linux 2.6.25 & Windows CE 6.0 R3 Operating Systems with complete BSP.

As part of the "Productized Services" program of e-con Systems, the eSOM300 is aimed at reducing the time-to-market for our customers by making use of the stabilized and ready-to-market eSOM300 modules in the customer applications. Being offered in SODIMM form factored modules with various configurations and OS support, these modules will enable our customers to focus on their application design rather than spending large unnecessary engineering man-hours involved in CPU/memory subsystem design.

Scope

The scope of this document is to detail all the technical details of the module from the hardware design perspective and mechanical design perspective. This document will serve as a single point of reference for hardware design of the customer application using eSOM300. This will provide the necessary details for the customers to integrate our eSOM300 with their application board design. The schematic designer and layout designer would find this document useful.

References

The reader of this document is also recommended to refer to the following documents for further details. The latest versions of these documents are available from the respective vendors.

- PXA300 Electrical, Mechanical and Thermal Specifications from Marvell Semiconductors
- PXA300 Family Design Manual from Marvell Semiconductors
- PXA300 Family Developer Manual Vol I, II, III and IV from Marvell Semiconductors

The following documents may also be referred to, though they may not be really required.

- Mircon Mobile DDR SDRAM datasheet from Micron
- NAND Flash memory datasheet from Numonyx

e-con highly recommends that the above manuals, especially the PXA300 CPU manuals are to be referred to before interfacing any peripheral with the eSOM300.

In addition to the above, e-con has made a wide range of documents such as hardware user manuals, BSP user/developer manuals, Driver API documents, sample

applications etc available for the customers to download. These documents also explain the basics of Windows CE application creation and debugging/profiling through KITL/ActiveSync, Windows CE kernel debugging/profiling though KITL, Linux Kernel debugging through kgdb etc. These Design Resources are aimed at reducing the head-start time for our customers and enable them to start using the modules the moment they receive the modules.

Description

The following sections describe the Hardware and Software features in detail.

1.1 Hardware

eSOM300 is a SODIMM sized CPU module designed and developed by e-con Systems. This CPU board is based on Marvell PXA300 Application Processor and contains mobile DDR DRAM, NAND Flash and Power Management IC. In addition eSOM300 offers a RTC, 10/100 MBit Ethernet as well as audio and touch-screen functionality. The 16 bit wide multiplexed system bus (DFI) is available for custom extensions. This module has been designed with SODIMM form factor with 204-pin SODIMM interface. This architecture makes it as a pluggable CPU board for a variety of target applications built around the base board on which it is plugged in to.

This CPU module is currently powered by Windows CE 6.0 and targeted to customers to reduce the Time-to-Market, by not worrying about the CPU subsystem, but to focus on the application base board design. This enables customers to build variety of base boards targeting various applications with a host of peripherals and interfaces, but keeping the CPU module standard which would be the work-horse of the entire product.

The module delivers state of the art technology, targeting low power systems that still require high CPU Performance. It also offers all the interfaces needed in a modern embedded device: besides the internal Flash Memory, there are several interfaces available for data storage such as NAND Flash and SD memory card. The CPU board also exposes the complete range of interfaces provided by the PXA300 Application Processor through its connectors so that the customers can get the complete functionality of PXA300, without going through the complex design requirements of the processor sub system including memory and power manager.

It also houses the Power Management IC, which can be programmed to change the core voltage to the CPU for DVM/DFM applications. The e-con's driver provides the API to change the core voltage and also boot level commands are provided for changing core voltage.

e-con also has a base board built around eSOM300 for evaluation. This development board will be available to customers with Board support packages, (incl. source code, on case to case basis) and other design inputs such as schematics and Bill of material (BOM) etc. The Development board has support for both Windows CE 6.0 and Linux 2.6.x. For additional details about the development board and a variety of add-on modules supported with eSOM300, please write to sales@e-consystems.com

1.2 Software

e-con provides the BSP for Windows CE 6.0 and Linux 2.6.x, with all the peripherals along with the development platform. Please contact e-con Systems for more information or other supported operating systems. sales@e-consystems.com

1.3 Features Summary

- Marvell XScale PXA300 @ 208/624 MHz
- 16 bit 64/128/256MB MOBILE DDR SDRAM - 1.8V ultra low power memory
- 8 bit 256/512/1024 MB NAND flash
- MAX8660 PMIC for PXA300
- Ethernet 10/100 MAC, only need to add magnetics/connector
- AC97 Audio codec with touch screen
- Inbuilt RTC
- Single Cell Li-ion Battery Charger
- SODIMM204 pin-out
- Comes with preinstalled u-boot.
- Programmable core voltage through I2C. u-boot commands are available for programming the core voltage
- Linux 2.6 support with source code

Block Diagram

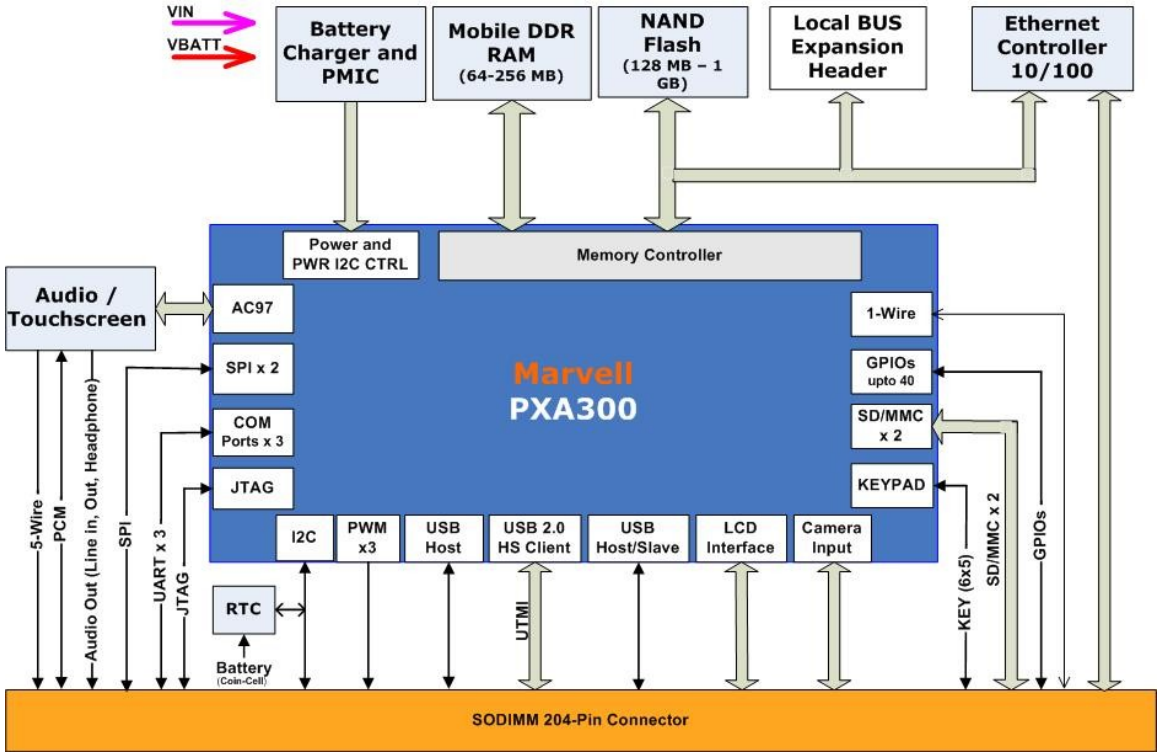

Fig 1: eSOM300 Block Diagram

Fig 1 shows the block diagram of eSOM300 interfaces, all the pins of eSOM300 mapped to multiple interfaces, all the interfaces can't be used simultaneously. The PMIC is MAX8660 from MAXIM-IC, is responsible for providing the power supply CPU as per the power-up requirements of the CPU and also powers the on-board MDDR, NAND Flash memory, Ethernet Controller and Audio codec.

The SYS_EN signal from the module is to be used by the application board designer to do the power sequencing required by the eSOM300 in accordance with their base board or base board peripherals. The Reset signals are available in the 204-pin connector for resetting the module from the application board.

Signal Description

This section describes signals grouped by their function. Each of the PXA300 has multiple functionalities other than the normal GPIO function. The GPIO pin can either be configured as one of the alternating functions or as a normal GPIO. The PXA300 contains lot of on-chip peripherals such as three UARTs, SD host controller, USB host controller, USB client controller, USB2.0 Client UTMI controller, LCD controller, Quick Capture Interface, PWM, I2C, SPI, AC97, etc. All these interfaces are taken out from eSOM300 and are grouped in the next section. These on-chip peripherals can work with different sets of GPIO pins with the proper alternate configuration or dedicated configuration.

For example, the KP_MKIN<0> signal (Matrix Key Pad signal) can be enabled by configuring either of the following GPIO pins: GPIO5, GPIO115. This flexibility of the PXA300 is to enable the customer to mix and match the GPIO signals to utilize the maximum number of on-chip peripherals. Please note that this flexibility is very limited and not all peripherals can be mapped to any GPIO. For example, the I2C signals are fixed on GPIO21 and GPIO22. This means, these GPIO pins can be either configured as I2C signals or as normal GPIO signals. No other functionality is possible. Please refer PXA300 Developer's Manual for more information and complete list of GPIO alternate functions configurations.

This document has a table of all the available on-chip peripheral interfaces the possibilities of how these peripherals can be mapped on to the GPIO pins. The following section explains the notation used in the tables below.

Item on the Table	Description of the item
Pin Name (Note1)	This item represents the Signal Name of the eSOM300 SODIMM connector (See Note1). The Signal Name is abbreviation of the signal functionality.
Description	This field describes the functionality of that signal. The description of the functionality is brief and hence please refers PXA300 Developer Manual for more detailed information and how to use that signal.
IO type	This field explains the I/O type of that signal. The values are explained as: I : Digital CMOS input O: Digital CMOS output IO: Digital CMOS Bidirectional Input/output

	PWR: Power supply or Ground pin
Multiplexed (Note2)	This field represents the multiplexing/configuration options of that signal. If this field is "Dedicated Pins", then, that signal(s) are dedicated for that usage cannot be configured. When this field has a group of GPIO pins, any one of these GPIO pins can be configured as that particular signal. When this field has only one GPIO pin, that pin can be configured as specified signal or that GPIO can be used as a normal GPIO, when that on-chip peripheral is not used. Please see PXA300 Developer Manual for more information. See the Note2 below.

Note1.

For dedicated pins are directly reflects the signal name in PIN NAME field, for GPIO pins, the required Signal Name functionality needs to configured by programming the alternate functions as required. .

Note2.

1. *For dedicated pins it is not applicable.*
2. *Some pins will be multiplexed with single GPIO; this can be configured for the required Signal Name functionality according to alternating function programmed for this GPIO*
3. *Some pins will have multiple GPIO for the same functionality and any one of these GPIO pins can be configured for the required Signal Name functionality; care should be taken while configuration of these pins.*

*The power domains of each signal are indicated in the l*ater section of the document. The application board (carrier board or base board) designer shall carefully go through the I/O signal configuration and its power domain before finalizing the connections. All the GPIO pins are powered inside the PXA300 at 3.3V in eSOM300 CPU Module. Please refer PXA300 manuals for more information about these power domains and the electrical parameters of the GPIO in each of the power domain.

1.4 Memory Bus

Pin Name	Description	IO type	Multiplexed
PXA_DF_IO [15…0]	Multiplexed AA/D to and from the external memory devices. The whole 16-bit interface can be used by the application board designer to support external memory bus peripherals such as Quad Uart Controller, USB Host Controller etc… after De-Mux Address and Data bus from DFI Bus.	IO	Dedicated Pins
PXA_DF_A [3…0]	Low-order address bits This can be used as the lowest four address bits during a burst transfer instead of the values in the lower address latch, this allows higher performance data transfer by avoiding most of the LLA cycles	O	Dedicated Pins
nPXA_DF_CLE_OE	Memory output enable	O	Dedicated Pins
nPXA_DF_ALE_WE	Memory Write enable	O	Dedicated Pins

nXCVREN	External Transceiver Enable	O	GPIO2
nPXA_LUA	Latch Upper Address	O	Dedicated Pins
nPXA_LLA	Latch Lower Address	O	Dedicated Pins
PXA_RDY	Variable latency VLIO signal for inserting wait states	I	Dedicated Pins
nCS0 nCS1	Static chip select: - These 2 chip select signals are available for the application board designer. These chip select signals have a fixed base address. The read/write timing parameters for each chip-select are individually programmable in memory configuration registers of PXA300.Please refer to PXA300 manuals for more details	O	Dedicated Pins

1.5 LCD Controller

Pin Name	Description	IO type	Multiplexed
LCD_DD [17:0]	LCD Display Data: Data lines used to transmit 4-, 8-, 16-, or 18-data values at a time to the LCD display module. Transfers pixel information from the LCD controller to the external LCD panel. These pins become inputs driven by the panel during a read from a panel with an integrated frame buffer. The LCD controller data line description changes with the type of LCD to be interfaced. Please refer to the PXA300 manual for more information.	IO	GPIO[71:54]
LCD_CS	LCD Chip Select: Chip select signal for LCD panels with an internal frame buffer.	O	GPIO15
LCD_FCLK	LCD Frame Clock: Frame clock used by the LCD display module to signal the start of a new frame of pixels that resets the line pointers to the top of the screen. This pin is also the vertical synchronization signal for active (TFT) displays. This pin is the read signal during reads from a panel with an internal frame buffers.	O	GPIO72
LCD_LCLK	LCD Line Clock: Indicates the start of a new line. Also referred to as H Sync (or horizontal synchronization) for active panels. For LCDs with an internal frame buffer, this signal indicates a command or data transaction.	O	GPIO73
LCD_PCLK	LCD Pixel Clock: Pixel clock used by the LCD display module to clock the pixel data into the line shift register. In passive mode, the pixel clock toggles only when valid data is available on the data pins. In active mode, the pixel clock toggles continuously, and the AC bias pin is used as an output to signal when data is valid on the LCD data pins. This pin also functions as a write signal for LCD panels with an internal frame buffer.	O	GPIO74

LCD_VSYNC	LCD Refresh Sync: Sync input driven by LCDs with an internal frame buffer	I	GPIO76
LCD_BIAS	LCD Bias Drive: AC bias that signals the LCD display module to switch the polarity of the power supplies to the row and column axis of the screen to counteract DC offset. In active (TFT) mode, it is used as the output enable to signal when data should be latched from the data pins using the pixel clock.	O	GPIO75

1.6 UARTS

1.6.1 Full-Function UART

Pin Name	Description	IO type	Multiplexed
UART1_RXD	Full-Function UART Receive Data	I	GPIO99 / 102 / 31 / 30 / 77 / 78 /100
UART1_TXD	Full-Function UART transmit Data	O	GPIO 100 / 31 30 / 77 / 78 / 99 / 102
UART1_CTS	Full-Function UART Clear-to-Send	I	GPIO 101 / 32 / 37 / 79 / 106
UART1_DCD	Full-Function UART Data-Carrier-Detects	I	GPIO 102 / 33 / 80
UART1_DSR	Full-Function UART Data-Set-Ready	I	GPIO 103 / 34 / 81 / 105
UART1_RI	Full-Function UART Ring Indicator	I	GPIO 104 / 35 / 82
UART1_DTR	Full-Function UART Data-Terminal-Ready	O	GPIO 105 / 34 / 36 / 81 / 103 /
UART1_RTS	Full-Function UART Request-to-Send	O	GPIO 106 / 32 / 37 / 79 / 101

1.6.2 Bluetooth UART

Pin Name	Description	IO type	Multiplexed
UART2_RXD	Bluetooth UART Receive Data	I	GPIO 112 / 19 / 18 / 113
UART2_TXD	Bluetooth UART transmit Data	O	GPIO 19 / 18 / 112 / 113
UART2_CTS	Bluetooth UART Clear-to-Send	I	GPIO 16 / 15 / 111 / 114
UART2_RTS	Bluetooth UART Data-Carrier-Detect	O	GPIO 16 / 15 / 111 / 114

Pin Name	Description	IO	Multiplexed

		type	
UART3_RXD	Bluetooth UART Receive Data	I	GPIO 7 / 8 / 94 / 93 / 110 / 109
UART3_TXD	Bluetooth UART transmit Data	O	GPIO 7 / 8 / 94 / 93 / 110 / 109
UART3_CTS	Bluetooth UART Clear-to-Send	I	GPIO 91 / 92 / 108 / 107
UART3_RTS	Bluetooth UART Data-Carrier-Detect	O	GPIO 91 / 92 / 108 / 107

1.7 Synchronous Serial Port (SSP)

Pin Name	Description	IO type	Multiplexed
SSP1_SCLK	Synchronous Serial Port 1 Clock: The serial bit-clock can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO85
SSP1_SFRM	Synchronous Serial Port 1 Frame: The serial frame sync can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO86
SSP1_TXD	Synchronous Serial Port 1 Transmit Data: Serial data driven out synchronously with the bit-clock.	O	GPIO87
SSP1_RXD	Synchronous Serial Port 1 Receive Data: Serial data latched using the bit-clock.	I	GPIO88
SSP1_EXT_CLK	Synchronous Serial Port 1 External Clock: This input supplies an external bit-clock or an external enable request for the internally generated bit-clock.	I	GPIO89
SSP1_SYS_CLK	Synchronous Serial Port 1 System Clock: When enabled, provides a reference clock at four times the port 1 bit-clock.	O	GPIO90
SSP3_SCLK	Synchronous Serial Port 3 Clock: The serial bit-clock can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO91
SSP3_SFRM	Synchronous Serial Port 3 Frame: The serial frame sync can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO92
SSP3_TXD	Synchronous Serial Port 3 Transmit Data: Serial data driven out synchronously with the bit-clock.	O	GPIO93
SSP3_RXD	Synchronous Serial Port 3 Receive Data: Serial data latched using the bit-clock.	I	GPIO94
SSP4_SCLK	Synchronous Serial Port 4 Clock: The serial bit-clock can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO95
SSP4_SFRM	Synchronous Serial Port 4 Frame: The serial	IO	GPIO96

	frame sync can be configured as an output (master-mode operation) or an input (slave-mode operation).		
SSP4_TXD	Synchronous Serial Port 4 Transmit Data: Serial data driven out synchronously with the bit-clock.	O	GPIO97
SSP4_RXD	Synchronous Serial Port 4 Receive Data: Serial data latched using the bit-clock.	I	GPIO98

1.8 USB

Pin Name	Description	IO type	Multiplexed
USBH1_P	USB Host Positive Line: Differential signal connects to the USB host interface.	IO (Analog)	Dedicated Pin
USBH1_N	USB Host Negative Line: Differential signal connects to the USB host interface.	IO (Analog)	Dedicated Pin
USB_HPWR	USB Host Power Indicator: Over-current indicator from USB power IC for USB host port.	I	GPIO1_2
USB_HPEN	USB Host Power Enable: Controls power IC for USB host port.	O	GPIO0_2
USBOTG_P	USB OTG Positive Line: Differential signal connects to the USB client interface.	IO (Analog)	Dedicated Pin
USBOTG_N	USB OTG Negative Line: Differential signal connects to the USB client interface.	IO (Analog)	Dedicated Pin

Pin Name	Description	IO type	Multiplexed
USB_P3_1	USB Full Speed Host Port 3 RCV	IO	GPIO 77
USB_P3_2	USB Full Speed Host Port 3 OE	IO	GPIO 78
USB_P3_3	USB Full Speed Host Port 3 RXD-	IO	GPIO79
USB_P3_4	USB Full Speed Host Port 3 TXD-	IO	GPIO80
USB_P3_5	USB Full Speed Host Port 3 RXD+	IO	GPIO81
USB_P3_6	USB Full Speed Host Port 3 TXD+	IO	GPIO82

Pin Name	Description	IO type	Multiplexed
UTM_DAT<0>	UTMI Data Bus	IO	GPIO 39 / 30
UTM_DAT<1>	UTMI Data Bus	IO	GPIO 40 / 31
UTM_DAT<2>	UTMI Data Bus	IO	GPIO 41 / 32
UTM_DAT<3>	UTMI Data Bus	IO	GPIO 42 / 33
UTM_DAT<4>	UTMI Data Bus	IO	GPIO 43 / 34
UTM_DAT<5>	UTMI Data Bus	IO	GPIO 44 / 35
UTM_DAT<6>	UTMI Data Bus	IO	GPIO 45 / 36
UTM_DAT<7>	UTMI Data Bus	IO	GPIO 46 / 37
UTM_CLK	UTMI Clock	I	GPIO 38
UTM_TXREADY	UTMI Transmit Data Ready	I	GPIO 53
UTM_RESET	UTMI Reset	O	GPIO 76 / 95 / 100
UTM_XCVR_SELECT	UTMI Transceiver Select	O	GPIO 64 / 96 /

			101 /
UTM_TERM_SELECT	UTMI Termination Select	O	GPIO 65 / 99 / 102
UTM_SUSPENDM	UTMI Suspend	O	GPIO 98 / 103 /
UTM_LINESTATE0	UTMI Line state 0	I	GPIO 109 / 92 / 104
UTM_LINESTATE1	UTMI Line state 1	I	GPIO 93 / 105
UTM_TXVALID	UTMI Transmit valid	O	GPIO 52 / 69 / 85
UTM_RXVALID	UTMI Receive data valid	I	GPIO 48 / 87 /
UTM_RXACTIVE	UTMI Receive Active	I	GPIO 49 / 47 / 88
UTM_RXERROR	UTMI Receive Error	O	GPIO 89
UTM_OPMODE0	UTMI Operating Mode 0	O	GPIO 51 / 90
UTM_OPMODE1	UTMI Operating Mode 1	O	GPIO 52 / 110 / 106

1.9 Quick Capture Interface

Pin Name	Description	IO type	Multiplexed
CIF_MCLK	Quick Capture Interface Master Clock: Programmable output Clock used by the camera capture sensor.	O	GPIO49
CIF_PCLK	Quick Capture Interface Pixel Clock: Pixel clock used by the quick capture interface of the camera to clock the pixel data into the input FIFO	I	GPIO50
CIF_DD0 CIF_DD1 CIF_DD2 CIF_DD3 CIF_DD4 CIF_DD5 CIF_DD6 CIF_DD7 CIF_DD8 CIF_DD9	Quick Capture Interface Data: Data lines to transmit 4, 5, 6,7,8,9 or 10 bits at a time. *Please refer to PXA300 developer manual for more details about the each pin description.*	I	GPIO39 GPIO40 GPIO41 GPIO42 GPIO43 GPIO44 GPIO45 GPIO46 GPIO47 GPIO48
CIF_HSYNC	Quick Capture Interface Frame Synchronization: Frame start or alternate synchronization signal used by the sensor to signal Frame read-out or as an external vertical synchronization.	IO	GPIO51
CIF_VSYNC	Quick Capture Interface Line Synchronization: Line start or alternate synchronization signal used by the sensor to signal line read-out or as an external horizontal synchronization	IO	GPIO52

1.10 MMC/SD Controller

Pin Name	Description	IO type	Multiplexed
MM1_CMD	MMC and SD Command	IO	GPIO14 / 8 / 15
MM1_DAT0	MMC Data 0	IO	GPIO3
MM1_DAT1	MMC Data 1	IO	GPIO4
MM1_DAT2	MMC Data 2	IO	GPIO5
MM1_DAT3	MMC Data 3	IO	GPIO6
MM1_CLK	MMC and SD Card Bus Clock	O	GPIO7

Pin Name	Description	IO type	Multiplexed
MM2_CMD	MMC and SD Command	IO	GPIO14 / 82
MM2_DAT0	MMC Data 0	IO	GPIO9 / 77
MM2_DAT1	MMC Data 1	IO	GPIO10
MM2_DAT2	MMC Data 2	IO	GPIO11 / 79
MM2_DAT3	MMC Data 3	IO	GPIO12 / 80
MM2_CLK	MMC and SD Card Bus Clock	O	GPIO13 / 81

1.11 I2C

Pin Name	Description	IO type	Multiplexed
PXA_I2C_SCL	I2C Clock: Serial clock.	IO	GPIO21
PXA_I2C_SDA	I2C Data: Serial data/address bus.	IO	GPIO22

1.12 PWM

Pin Name	Description	IO type	Multiplexed
PWM0	Pulse Width Modulation Channel 0	O	GPIO17
PWM1	Pulse Width Modulation Channel 1	O	GPIO18
PWM2	Pulse Width Modulation Channel 2	O	GPIO19

1.13 KEY PAD

Pin Name	Description	IO type	Multiplexed
KP_MKOUT<0>	Matrix Key Scan Lines	O	GPIO121 / 85
KP_MKOUT<1>	Matrix Key Scan Lines	O	GPIO122 / 86
KP_MKOUT<2>	Matrix Key Scan Lines	O	GPIO123 / 87
KP_MKOUT<3>	Matrix Key Scan Lines	O	GPIO124 / 88
KP_MKOUT<4>	Matrix Key Scan Lines	O	GPIO125 / 19
KP_MKOUT<5>	Matrix Key Scan Lines	O	GPIO7 / 11 / 38
KP_MKIN<0>	Matrix Key Return Lines	I	GPIO115 / 5

KP_MKIN<1>	Matrix Key Return Lines	I	GPIO116 / 6
KP_MKIN<2>	Matrix Key Return Lines	I	GPIO117
KP_MKIN<3>	Matrix Key Return Lines	I	GPIO118
KP_MKIN<4>	Matrix Key Return Lines	I	GPIO119
KP_MKIN<5>	Matrix Key Return Lines	I	GPIO120

1.14 JTAG

Pin Name	Description	IO type	Multiplexed
JTAG_nTRST	JTAG Test Reset: IEEE 1194.1 test reset.	I	Dedicated Pin
JTAG_TDI	JTAG Test Data Input: Data from the JTAG controller is sent to the PXA3xx processor using this signal. This pin has an internal pullup Resistor.	I	Dedicated Pin
JTAG_TDO	JTAG Test Data Output: Data from the PXA3xx processor is Returned to the JTAG controller using this signal.	O	Dedicated Pin
JTAG_TMS	JTAG Test Mode Select: Selects the test mode required from the JTAG controller. This pin has an internal pull-up resistor.	I	Dedicated Pin
JTAG_TCK	JTAG Test Clock: For all transfers on the JTAG test interface.	I	Dedicated Pin
VCC_JTAG	VCC to be used only for JTAG connector	PWR	Dedicated Pin

1.15 Ethernet Signals

Pin Name	Description	IO type	Multiplexed
{ ETH_TPO+, ETH_TPO- }	Transmit Differential Pair. The transmit differential pair sends serial bit streams to the unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T (Manchester) mode and a three-level signal in 100BASE-TX mode (MLT-3). These signals interface directly with the isolation transformer	O	Dedicated Pin
{ ETH_TPI+, ETH_TPI- }	Receive Differential Pair. The receive differential pair receives the serial bit stream from an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals interface directly with an isolation	I	Dedicated Pin

	transformer		
ETH_LK_ACT	Link Status/Active: If this signal is low, it indicates link, and if it is high, then the link is fail. When in link status and line activity occurrence, this signal is pulsed high (LED off) for 80ms whenever transmit or receive activity is detected. This signal is then driven low again for a minimum of 80ms, after which time it will repeat the process if TX or RX activity is detected	O	Dedicated Pin
ETH_SPEED	Speed Status: If this signal is low, it indicates 100Mbps, and if it is high, then the speed is 10Mbps	O	Dedicated Pin

1.16 Audio Codec Signals

Pin Name	Description	IO type	Multiplexed
LINE_IN_L	Left Line Input	AI	Dedicated Pin
LINE_IN_R	Right Line Input	AI	Dedicated Pin
MIC2A	Microphone preamp A input 2	AI	Dedicated Pin
MIC2B	Microphone preamp B input	AI	Dedicated Pin
MIC_CM	Microphone common mode input	AI	Dedicated Pin
MICBIAS	Bias voltage for Microphones	AO	Dedicated Pin
LINE_OUT_L	Left Speaker Line Out	AO	Dedicated Pin
LINE_OUT_R	Right Speaker Line Out	AO	Dedicated Pin
HP_OUT_L	Left Head phone Line Out	AO	Dedicated Pin
HP_OUT_R	Right Head phone Line Out	AO	Dedicated Pin
MONO_SPK_OUT	Mono output driver	AO	Dedicated Pin

Pin Name	Description	IO type	Multiplexed
PCM_CLK	PCM interface clock	I	Dedicated Pin
PCM_FS	PCM Frame Signal	I	Dedicated Pin
PCM_DAC	PCM input (DAC) data	IO	Dedicated Pin
PCM_ADC	PCM output (ADC) data	IO	Dedicated Pin

1.17 TSC Signals

Pin Name	Description	IO type	Multiplexed
TSC_X+	Touch panel connection: X+ (Right)	AI	Dedicated Pin
TSC_X-	Touch panel connection: X- (Left)	AI	Dedicated Pin
TSC_Y+	Touch panel connection: Y+ (Top)	AI	Dedicated Pin
TSC_Y-	Touch panel connection: Y- (Bottom)	AI	Dedicated Pin
TSC_WIPER	Touch sheet connection for 5-wire Touch panel	AI	Dedicated Pin

1.18 Power Sequencing and Reset

Pin Name	Description	IO type	Multiplexed
nMR_PMIC_RESET	Reset Input	I	Dedicated Pin
nPXA_RST_OUT	Reset Out: Indicates to the system that the PXA3xx processor family is in a reset state.	O	Dedicated Pin
PXA_SYS_EN	System Enable for System Peripheral Power Supply.	O	Dedicated Pin

1.19 Power

Pin Name	Description	IO type	Multiplexed
VCC_IN	Main power supply, connect to 5V	PWR	Dedicated Pin
VCC_BAT*	Connect this pin to Single Cell Li-ion Battery (4.2V)	PWR	Dedicated Pin
GND	Main Ground	PWR	Dedicated Pin

* Available in eSOM300 with Battery Charger Configuration

1.20 Power Specifications

1.20.1 Power Consumption

Absolute maximum ratings

Description	Max	Unit	Conditions
Power dissipation of the eSOM300	2.5	W	• PXA300 Operated at 624mhz • LCD Controller Enabled • FTP File transfer through Ethernet • File transfer through (UTMI) USB2.0 client • Running Transcriber Application • **Without Battery Charger**

Note5: input power should be designed to meet the above specification and e-con recommends the input power supply should be designed for 2.5W at 5V.

1.20.2 Power-up sequence

The sequence for power is as follows:

1. VCC_IN (5V) is to be established first from the application board before powering any other power supply inputs.

2. The application board peripherals power must be established after processor asserts the SYS_EN high.

eSOM300 Connector details

Item on the Table	Description of the item
SODIMM Pin Number	This Field represents the Pin number of the SODIMM connector used in BASE BOARD of eSOM300 module.
Signal Name	This field describes the signal name of the pin number of eSOM300. Please refer PXA300 Developer Manual for more detailed information and how to use that signal.
Supply Assigned	This signal mentioned in the second field, is assigned to the power mentioned in this field. Please refer PXA300 Developer Manual for more detailed information and how to use that signal with power supply mentioned.
Internal Power Domain	Signal mentioned in second field belongs to the this supply domain .For More details refer PXA300 Developer Manual

1.21 SODIMM Connector Pinout

SODIMM Pin Number	Signal Name	Voltage Logic	Internal Power Domain	SODIMM Pin Number	Signal	Voltage Logic	Internal Power Domain
1	ETH_TPO+	3P3V		2	ETH_TPI+	3P3V	
3	ETH_TPO-	3P3V		4	ETH_TPI-	3P3V	
5	ETH_SPEED	3P3V		6	ETH_LK_ACT	3P3V	
7	GND			8	GND		
9	LINE_IN_L	3P3V		10	MIC_CM	3P3V	
11	LINE_IN_R	3P3V		12	TSC_WIPER	3P3V	
13	MICBIAS	3P3V		14	TSC_X+	3P3V	
15	MIC2A	3P3V		16	TSC_Y+	3P3V	
17	MIC2B	3P3V		18	TSC_X-	3P3V	

19	GND	3P3V	
21	LINE_OUT_L	3P3V	
23	LINE_OUT_R	3P3V	
25	HP_OUT_L	3P3V	
27	HP_OUT_R	3P3V	
29	GND		
31	GPIO16	3P3V	VCC_CARD2
33	GPIO17	3P3V	VCC_IO3
35	GPIO19	3P3V	VCC_IO3
37	GPIO14	3P3V	VCC_CARD2
39	GPIO13	3P3V	VCC_CARD2
41	GPIO12	3P3V	VCC_CARD2
43	GPIO9	3P3V	VCC_CARD2
45	GPIO10	3P3V	VCC_CARD2
47	GPIO11	3P3V	VCC_CARD2
49	GPIO31	3P3V	VCC_IO3

20	TSC_Y-	3P3V	
22	MONO_SPK_OUT	3P3V	
24	GND		
26	PCM_CLK	3P3V	
28	PCM_FS	3P3V	
30	PCM_DAC	3P3V	
32	PCM_ADC	3P3V	
34	nPXA_CS1	3P3V	VCC_DF
36	nPXA_CS0	3P3V	VCC_DF
38	GPIO3	3P3V	VCC_CARD1
40	GPIO4	3P3V	VCC_CARD1
42	GPIO5	3P3V	VCC_CARD1
44	GPIO6	3P3V	VCC_CARD1
46	GPIO7	3P3V	VCC_CARD1
48	GPIO8	3P3V	VCC_CARD1
50	GPIO22	3P3V	VCC_IO3

SODIMM Pin Number	Signal Name	Voltage Logic	Internal Power Domain
51	GPIO32	3P3V	VCC_IO3
53	GPIO33	3P3V	VCC_IO3
55	GPIO34	3P3V	VCC_IO3
57	GPIO36	3P3V	VCC_IO3
59	GPIO38	3P3V	VCC_IO3
61	GND		
63	GPIO40	3P3V	VCC_CI
65	GPIO44	3P3V	VCC_CI
67	GPIO46	3P3V	VCC_CI
69	GPIO45	3P3V	VCC_CI
71	GPIO42	3P3V	VCC_CI
73	GPIO50	3P3V	VCC_CI

SODIMM Pin Number	Signal	Voltage Logic	Internal Power Domain
52	GPIO21	3P3V	VCC_IO3
54	GPIO30	3P3V	VCC_IO3
56	GPIO35	3P3V	VCC_IO3
58	GPIO37	3P3V	VCC_IO3
60	NC		
62	NC		
64	NC		
66	GPIO39	3P3V	VCC_CI
68	GPIO41	3P3V	VCC_CI
70	GPIO43	3P3V	VCC_CI
72	GPIO47	3P3V	VCC_CI
74	GPIO48	3P3V	VCC_CI

75	GPIO51	3P3V	VCC_CI
77	GPIO18	3P3V	VCC_IO3
79	GPIO15	3P3V	VCC_CARD2
81	GPIO54	3P3V	VCC_LCD
83	GPIO56	3P3V	VCC_LCD
85	GPIO58	3P3V	VCC_LCD
87	GPIO60	3P3V	VCC_LCD
89	GPIO62	3P3V	VCC_LCD
91	GPIO64	3P3V	VCC_LCD
93	GPIO66	3P3V	VCC_LCD
95	GPIO68	3P3V	VCC_LCD
97	GPIO70	3P3V	VCC_LCD
99	GND		

76	GPIO49	3P3V	VCC_CI
78	GPIO52	3P3V	VCC_CI
80	GND		
82	GPIO55	3P3V	VCC_LCD
84	GPIO57	3P3V	VCC_LCD
86	GPIO59	3P3V	VCC_LCD
88	GPIO61	3P3V	VCC_LCD
90	GPIO63	3P3V	VCC_LCD
92	GPIO65	3P3V	VCC_LCD
94	GPIO67	3P3V	VCC_LCD
96	GPIO69	3P3V	VCC_LCD
98	GPIO71	3P3V	VCC_LCD
100	GPIO73	3P3V	VCC_LCD

SODIMM Pin Number	Signal Name	Voltage Logic	Internal Power Domain
101	GPIO74	3P3V	VCC_LCD
103	GPIO72	3P3V	VCC_LCD
105	GPIO75	3P3V	VCC_LCD
107	GPIO8_2	3P3V	
109	GPIO7_2	3P3V	
111	NC		
113	NC		
115	GPIO85	3P3V	VCC_MSL
117	GPIO88	3P3V	VCC_MSL
119	GPIO90	3P3V	VCC_MSL
121	GPIO86	3P3V	VCC_MSL
123	GPIO87	3P3V	VCC_MSL
125	GPIO89	3P3V	VCC_MSL
127	GPIO97	3P3V	VCC_IO1

SODIMM Pin Number	Signal	Voltage Logic	Internal Power Domain
102	GPIO76	3P3V	VCC_LCD
104	GND		
106	GPIO77	3P3V	VCC_MSL
108	GPIO78	3P3V	VCC_MSL
110	GPIO79	3P3V	VCC_MSL
112	GPIO80	3P3V	VCC_MSL
114	GPIO81	3P3V	VCC_MSL
116	GPIO82	3P3V	VCC_MSL
118	GPIO94	3P3V	VCC_IO1
120	GPIO93	3P3V	VCC_IO1
122	GPIO91	3P3V	VCC_IO1
124	GPIO92	3P3V	VCC_IO1
126	GPIO95	3P3V	VCC_IO1
128	GPIO96	3P3V	VCC_IO1

129	GPIO98	3P3V	VCC_IO1
131	GPIO115	3P3V	VCC_IO1
133	GPIO116	3P3V	VCC_IO1
135	GPIO117	3P3V	VCC_IO1
137	GPIO118	3P3V	VCC_IO1
139	GPIO119	3P3V	VCC_IO1
141	GPIO120	3P3V	VCC_IO1
143	USBOTG_P	3P3V	VCC_BIAS
145	USBOTG_N	3P3V	VCC_BIAS
147	GND		
149	GPIO99	3P3V	VCC_IO1

130	GPIO121	3P3V	VCC_IO1
132	GPIO122	3P3V	VCC_IO1
134	GPIO123	3P3V	VCC_IO1
136	GPIO124	3P3V	VCC_IO1
138	GPIO125	3P3V	VCC_IO1
140	GND		
142	USBH1_P	3P3V	VCC_BIAS
144	USBH1_N	3P3V	VCC_BIAS
146	GPIO100	3P3V	VCC_IO1
148	GPIO106	3P3V	VCC_IO1
150	GPIO101	3P3V	VCC_IO1

SODIMM Pin Number	Signal Name	Voltage Logic	Internal Power Domain
151	GPIO102	3P3V	VCC_IO1
153	GPIO103	3P3V	VCC_IO1
155	GPIO53	3P3V	VCC_LCD
157	GPIO104	3P3V	VCC_IO1
159	GPIO112	3P3V	VCC_IO1
161	GPIO113	3P3V	VCC_IO1
163	GPIO111	3P3V	VCC_IO1
165	GPIO114	3P3V	VCC_IO1
167	GPIO105	3P3V	VCC_IO1
169	EXT_WKUP0	3P3V	VCC_BBATT
171	NC		
173	JTAG_TMS	3P3V	VCC_BBATT
175	JTAG_TDO	3P3V	VCC_BBATT
177	VBAT_RTC	3P3V	VCC_BBATT
179	nPXA_RST_OUT	3P3V	
181	BAT_TEMP_SEN	3P3V	

SODIMM Pin Number	Signal	Voltage Logic	Internal Power Domain
152	GPIO126	3P3V	VCC_IO1
154	GPIO1_2	3P3V	VCC_IO1
156	GPIO0_2	3P3V	VCC_IO1
158	GPIO110	3P3V	VCC_IO1
160	GPIO109	3P3V	VCC_IO1
162	GPIO108	3P3V	VCC_IO1
164	GPIO107	3P3V	VCC_IO1
166	GND		VCC_IO1
168	JTAG_nTRST	3P3V	VCC_BBATT
170	JTAG_TCK	3P3V	VCC_BBATT
172	JTAG_TDI	3P3V	VCC_BBATT
174	PXA_SYS_EN	3P3V	VCC_BBATT
176	nMR_PMIC_RESET	3P3V	VCC_BBATT
178	VCC_JTAG	3P3V	VCC_BBATT
180	CHR_PEN1	3P3V	
182	nBAT_CHG_DONE	3P3V	

183	BAT_ISET	3P3V	
185	GND		
187	GND		
189	GND		
191	VCC_BAT		
193	VCC_BAT		
195	VCC_BAT		
197	VCC_BAT		
199	VCC_BAT		
201	VCC_BAT		
203	VCC_BAT		

184	nBAT_CHG_STAT	3P3V	
186	GND		
188	GND		
190	GND		
192	VCC_IN		
194	VCC_IN		
196	VCC_IN		
198	VCC_IN		
200	VCC_IN		
202	VCC_IN		
204	VCC_IN		

1.22 FPC (1 x 30-Pin) DFI Bus Connector

Top side (e-con logo)			
FPC Pin Number	**Signal Name**	**Supply assigned**	**Internal Power Domain**
1	GND		
2	PXA_DF_IO0	3P3V	VCC_DF
3	PXA_DF_IO1	3P3V	VCC_DF
4	PXA_DF_IO2	3P3V	VCC_DF
5	PXA_DF_IO3	3P3V	VCC_DF
6	PXA_DF_IO4	3P3V	VCC_DF
7	PXA_DF_IO5	3P3V	VCC_DF
8	PXA_DF_IO6	3P3V	VCC_DF
9	PXA_DF_IO7	3P3V	VCC_DF
10	GND		
11	PXA_DF_IO8	3P3V	VCC_DF
12	PXA_DF_IO9	3P3V	VCC_DF
13	PXA_DF_IO10	3P3V	VCC_DF
14	PXA_DF_IO11	3P3V	VCC_DF
15	PXA_DF_IO12	3P3V	VCC_DF
16	PXA_DF_IO13	3P3V	VCC_DF

17	PXA_DF_IO14	3P3V	VCC_DF
18	PXA_DF_IO15	3P3V	VCC_DF
19	nPXA_DF_CLE_OE	3P3V	VCC_DF
20	nPXA_DF_ALE_WE	3P3V	VCC_DF
21	GND		
22	nXCVREN	3P3V	VCC_DF
23	PXA_RDY	3P3V	VCC_DF
24	nPXA_LUA	3P3V	VCC_DF
25	nPXA_LLA	3P3V	VCC_DF
26	PXA_DF_A3	3P3V	VCC_DF
27	PXA_DF_A2	3P3V	VCC_DF
28	PXA_DF_A1	3P3V	VCC_DF
29	PXA_DF_A0	3P3V	VCC_DF
30	GND		

Technical Specifications

1.23 Electrical – DC Characteristics

1.23.1 Supply Voltage

Supply	Description	Min	Typ	Max	Unit
VCC_IN	Main Supply voltage for Battery Charger/PMIC	4.5	5	6.0	V
VCC_BAT	Input Supply voltage from Battery	3.6	-	4.2	V

1.23.2 Operating Current

The operating current is measured with the supply voltage of 5V with the following operating scenarios. eSOM300 configuration considered for power consumption estimation is 624MHz Core clock, 256MB MOBILE DDR SDRAM, 256MB Flash and core voltage 1.45V.

Supply	Condition	Typical Current	Unit
VCC_IN = 5V	• PXA300 Operated at 624MHz • LCD Controller Enabled • FTP File transfer through Ethernet • File transfer through (UTMI) USB2.0 client • Running Touch Transcriber Application • **Without Battery Charger** • Ambient Temperature at 25°C	350	mA

1.24 IO Voltage level

VIH	High level input voltage, applicable to all standard input and IO pins (VCC_IO, VCC_MEM, VCC_DF, VCC_LCD, VCC_BIAS,VCC_MSL,VCC_CI,VCC_CARD1 or VCC_CARD2)	VCC -0.3	VCC	V(Note8)
VIL	Low level input voltage, applicable to all standard input and IO pins (VCC_IO, VCC_MEM, VCC_DF, VCC_LCD, VCC_BIAS,VCC_MSL,VCC_CI,VCC_CARD1 or VCC_CARD2)	GND-0.1	0.2*VCC	V
VOH	High level output voltage applicable to all standard input and IO pins(VCC_IO, VCC_MEM, VCC_DF, VCC_LCD, VCC_BIAS,VCC_MSL,VCC_CI,VCC_CARD1 or VCC_CARD2)	VCC-0.3	VCC	V(Note8)
VOL	Low level output voltage applicable to all standard input and IO pins(VCC_IO, VCC_MEM, VCC_DF, VCC_LCD, VCC_BIAS,VCC_MSL,VCC_CI,VCC_CARD1 or VCC_CARD2)	GND	VSS+0.3	V(Note8)

Note 8: VCC corresponds to individual power domain to which the signal is internally connected to. This individual power domain for each signal is listed in the previous sections of this document. In eSOM300 all the IO lines are operating at VCC=3.3V.

1.25 Memory Map

Description	Range
Chip select 0	0x0000 0000 – 0x0FFF FFFF
Chip select 1	0x3000 0000 – 0x3FFF FFFF

1.26 Temperature Range*

Description	Min	MAX	Unit
Operating Temperature of eSOM300 (Ambient)*	-25	+85	°C

*Note: Applicable only when modules are ordered with extended temp otherwise commercial temperature applicable (0 °C to 70 °C)

1.27 Mechanical

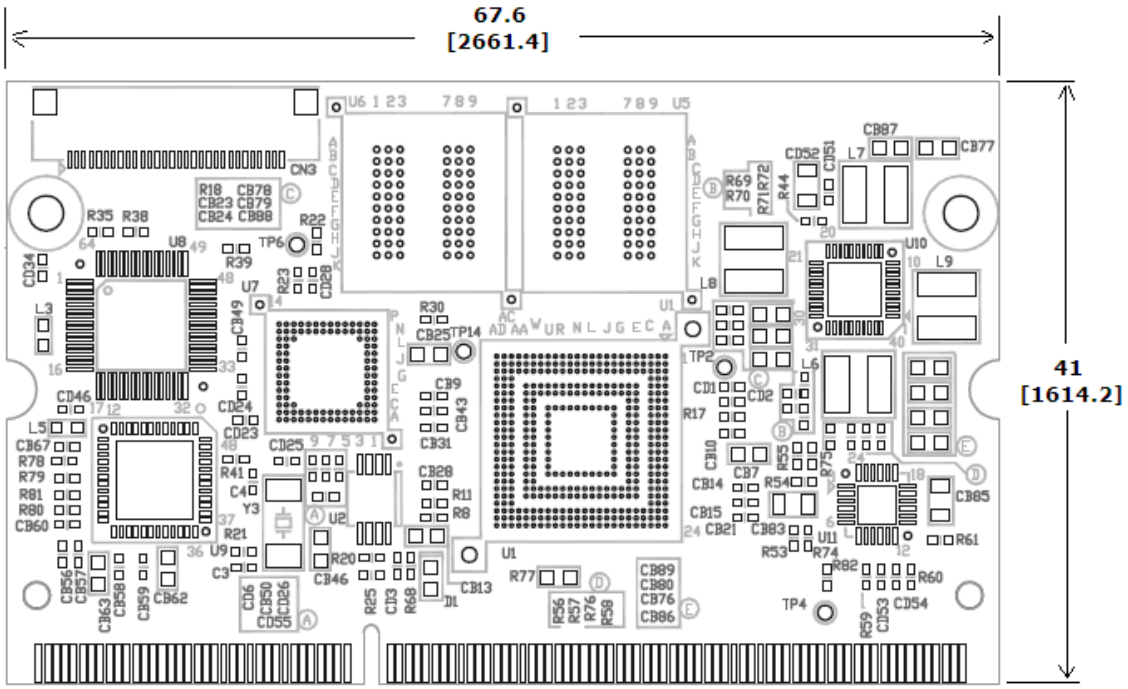

Fig shows the mechanical dimensions of the eSOM300 module.

Note: Dimension in mm [mils]

For more details, please refer eSOM300 dxf file.

1.27.1 Sockets for the eSOM300 Module

eSOM300 fits into standard 1.5V DDR3 SODIMM204 pin connector; the details of the connector are given below.

Manufacturer	Molex
Manufacturer Part number	78121-0001
Description	CONN SODIMM DDR3 204POS R/A SMD

1.27.2 Ordering information

Please refer to the eSOM300 Configuration document or visit
www.e-consystems.com/eSOM300.asp

1.27.3 RoHS Compliance

e-con Systems adheres to the RoHS directives and ensures that all the products designed and manufactured by e-con Systems in full compliance with Restriction of Hazardous Substance (RoHS). Please contact sales@e-consystems.com for more information.

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